IN THE CLAIMS

1. (Canceled).

2. (Currently Amended) A multiprocessor machine ~~as described in claim 1 further~~ comprising: a plurality of processors; a first cache shared by said plurality of processors; and a first controller providing control so that data accessed by at least two processors out of said plurality of processors is given higher priority in being saved to said first cache compared to data accessed by only one of said plurality of processors;

second caches associated with each of said plurality of processors; and a second controller providing control so that, when data stored in a second cache is accessed by a processor other than a processor associated with said second cache, said data is not stored in said second cache with a higher priority compared to data accessed only by said processor associated with said second cache.

3. (Canceled).

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~~4~~. (Original) A multiprocessor machine as described in
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claim ~~2~~ wherein said plurality of processors and said first cache and said controller and said second cache and said second controller are integrated on a single LSI.

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~~5~~. (Currently Amended) A multiprocessor machine ~~as described in claim 1~~ comprising: a plurality of processors; a first cache shared by said plurality of processors; and a first controller providing control so that data accessed by at least two processors out of said plurality of processors is given higher priority in being saved to said first cache compared to data accessed by only one of said plurality of processors,

wherein said first controller includes first selecting means which, if storing new data to said first cache and there is an area in said first cache containing data not accessed by at least two processors of aid plurality of processors, selects said area in said first cache over an area containing data accessed by at least two processors of said plurality of processors.

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6. (Original) A multiprocessor machine as described in claim 1 wherein said second controller includes second selecting means which, if storing new data to said second cache and there is an area in said second cache containing data accessed by a processor other than a processor associated with said second cache, selects said area in said second cache over an area containing data accessed by only said processor associated with said second cache.

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7. (Original) A method for controlling cache comprising:

a first step evaluating whether data stored in a cache shared by a plurality of processors is accessed by at least two processors from said plurality of processors;

a second step selecting an area determined by said first step to not be accessed by at least two processors when storing new data to said cache;

a third step selecting an area in said cache if no area can be selected in said second step; and

a fourth step storing said new data in said cache area selected by either said second step or said third step.

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8. (Original) A method for controlling cache as described in claim 5 wherein said third step selects an area containing data with the lowest number of accessing processors.

9. (Canceled).

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10. (Original) A processor system comprising: a plurality of processors; a cache memory accessible by at least two processors of said plurality of processors; a first bus connecting said plurality of processors and said cache memory; a main storage memory exchanging data with said cache memory; a second bus connecting said cache memory and said main storage memory; a sharing evaluation module evaluating whether data stored in said cache memory is accessed by at least two processors and adding attributes to said data; and a replacement controller selecting data in said cache memory determined to not be accessed by at least two processors based on said attributes over data determined to be accessed by at

least two processors, and replacing data in said main storage memory with said selected data.

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~~11~~. (Original) A processor system as described in claim 7
~~10~~ wherein said cache memory includes a plurality of sets, said sets containing information indicating whether data in said sets is use by a plurality of processors.

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~~12~~. (Original) A processor system as described in claim 8
~~11~~ wherein said sets include information indicating validity of data and information indicating whether data was rewritten.

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~~13~~. (Original) A processor system as described in claim 9
~~12~~ wherein said sets include an identifier of a processor that last accessed said data.

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~~14~~. (Original) A processor system as described in claim 10
~~13~~ wherein said replacement controller selects an area of said cache memory to replace data in said main storage memory based on said information indicating whether data in said set is use by a plurality of processors, said information indicating

validity of data, and said information indicating whether data was rewritten.